Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: Cr-Ni / V-Ag**

**Bond Pad Size: Gate = .030” X .033”**

**Backside Potential: Collector**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .170” X .232” DATE: 8/30/21**

**MFG: IR THICKNESS .015” P/N: IRG4BC40W**

**DG 10.1.2**

#### Rev B, 7/19/02